Systolic Signal Processing Research Group Activity

Ewa Lipowska-Nadolska, Sławomir Klimczak, Marcin Kwapisz, Krzysztof Lichy

***Abstract* — This paper presents projects concerning systolic signal processing that are led by Ewa Lipowska-Nadolska in Division of Computer Networks, Technical University of Łódź**

I. Project 1 - Image compression using systolic arrays [1-7].

A goal of this research project is an application of systolic arrays for image compression, especially for one of its stage - discrete wavelet transform (DWT).

For research purposes an MS Windows application was written to compare DWT sequential algorithms to DWT systolic algorithms. There are compared parameters like:

1. Compression ratio.
2. Original signal distortion.
3. Efficiency (computation time).

User can also set the following parameters:

- Kind of an algorithm: convolution, matrix, lift.
- Data type: real-to-real, integer-to-integer
- Realization: hardware (systolic array), software
- Tile size (in pixels): 32, 64, 128, 256, 512
- Decomposition level: I, II, III, IV

Systolic algorithms were created for mentioned above kinds of algorithms and they were adopted to systolic computer SYSTOLA 1024.

A. Convolution:

Columns and rows of an image are convolved with coefficients of DWT filter. There are many linear systolic arrays for solving convolution. Our goal was to compute convolution on orthogonal systolic array and to increase overall algorithm performance.

B. Matrix:

This method uses matrix-matrix multiplication to compute DWT. One matrix is an image part (one tile) and the second is matrix of DWT coefficients.

SYSTOLA 1024 is a perfect tool for this method because it has been designed for such kind of algorithms. We had to create for this method sets of filter banks for different DWTs.

C. Lift:

Sequential algorithm for Lift method is very efficient. It exploits prediction and update of computed data values. We had to adopt and convert "lift algorithm" for systolic array.

Results of this project are:

1. SYSTOLA 1024 can by used to perform DWT computations.
2. All mentioned algorithms can be transformed to systolic algorithms.
3. These algorithms can be optimized for better performance.

II. Project 2 - Design of systolic arrays architectures [4-5][9-11][14]

The main objective of this project was to write CAD-like software that helps a user to design and verify systolic arrays architecture. Following assumptions were taken in this project:

1. Algorithm is given in dependence graph (DG) form.
2. All graphs are described in 3D vector space.
3. Transform process from DG to final systolic architecture has to be parameterized.
4. Final systolic array architecture can be verified by simulation (using any set of input data)

The result of this project is a MS Windows application that fulfill assumptions 1 to 4.

Ad. 1 The first step is to create DG for given algorithm. All nodes of DG have to be identical (homogeneous DG) and functions being bound up with node arcs have to be defined.

Ad. 2 Node position and arcs joining neighbouring nodes are described by 3D vector class. Therefore user can create DGs in up to three dimensional space (2D and 3D graphs are possible)

Ad. 3 Algorithms described in [8][15][16] are used to transform DG to final systolic array architecture. A few adjustments were needed to adapt them to the application. Author's original algorithms are also implemented. They are used to parameterized the transformation to achieve systolic array architecture with desired properties like:

a) 1D (e.g.: linear, ring) systolic array or 2D (e.g.: orthogonal, planar, cylindrical) systolic array - shape property.
b) Minimum processing elements (PE) count - size property.
c) Maximum efficiency - efficiency property
d) Effectiveness (PE usage during systolic computations) - efficiency property.

User can set his own parameters or he can choose the application to compute optimal parameters for him automatically. In the second case user has to select one of four foregoing properties (properties a to d) but he is not able to control transformation of DG and introduce corrections on each transformation stage.

Authors represent Division of Computer Networks, Technical University of Łódź, ul. Stefanowskiego 18/22, 90-537 Łódź, Poland, e-mail: eln@zsk.p.lodz.pl, klimek@zskl.zsk.p.lodz.pl, mkwapisz@zskl.zsk.p.lodz.pl, lichy@zskl.zsk.p.lodz.pl

All time-space data dependencies of a systolic algorithm are computed during transformation of DG to systolic array architecture. Functions bound up with node arcs are joined and converted to one computational procedure of PE.

Ad. 4 Special simulation module has been implemented in the application. Final systolic array can be verified using any set of data in matrix or vector form. This form is required by general systolic array properties. User do not have to compute additional delays in input data because it is done during transformation of DG. During simulation all computations are performed as it was real systolic array, so user can see, write to disk and analyze state of systolic array in each subsequent pulsation.

An original contribution of this project is:

1. The CAD-like application to design systolic arrays architectures.
2. Systolic array architectures designs created with the application for such algorithms as: processing of 1D and 2D signals (e.g. matrix algebra, filtering, discrete transforms), computational intelligence algorithms (artificial neural networks - ANN and genetic algorithms - GA).

III. PROJECT 3 - SYSTOLIC IMPLEMENTATION OF MORPHOLOGICAL PROCESSING [15-16]

Term morphology means the scientific study of the form and structure of animals and plants. In context of image processing this term means studying of topology or structure of objects from their images. Morphological processing refers to certain operation where an object is hit with a structuring element and as a result an image is converted to more revealing shape. Morphological processing was originally discovered by G.Matheron and J.Serre from " Ecole des Mines de Paris" in the 1960.

Mathematical morphology on the pictures are current and future topic of research. They can be used in the widely spread recognition of pattern in the picture. There are a lot of practical usages for example in picture analysis. Morphological filter allows for fast searching of the shape in the picture which can be implemented in a lot of practical usages such as for example: computer tomography or rummage of the databases with fingerprints additionally in analyzing of DNA. Considering its orthogonal architecture (32x32 processors) Systola 1024 is very good for performing morphological operations.

The idea of systolic array is an original treatment to the question how to design hardware fit tight for a concrete calculation problem. The systolic time-space algorithms fit tightly the hardware architecture are perfect tools to execute morphological operations on the picture.

The original contribution of these project of will be treatise of time-space algorithms for mathematical morphology and their verification on Systola 1024, one of two which are in Poland.

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